CLAIMS

1. A signal modulation circuit for modulating a differential pulse width modulation signal, comprising:
a first channel signal processing element having an input coupled for receiving a first channel of the differential signal, an output, and a control signal output;
a second channel signal processing element having an input coupled for receiving a second channel of the differential signal, an output, and a control signal output;
a first logic gate having a first input coupled to the output of said first channel signal processing element, a second input coupled to the output of said second channel signal processing element, and an output;
a second logic gate having a first input coupled to the control signal output of said first channel signal processing element, a second input coupled to the control signal output of said second channel signal processing element, a third input coupled to the output of said first logic gate, and an output;
a first switch having a first electrode coupled to the output of said first channel signal processing element, a second electrode coupled for transmitting a first channel of an output signal, and a control electrode coupled to the output of said second logic gate; and
a second switch having a first electrode coupled to the output of said second channel signal processing element, a second electrode coupled for transmitting a second channel of the output signal, and a control electrode coupled to the output of said second logic gate.

2. The signal modulation circuit of claim 1, wherein:
said first switch includes a first logic AND gate having a first input coupled to the output of said first channel signal processing element, a second input coupled to the output of said second logic gate, and an output coupled for transmitting the first channel of the output signal; and
said second switch includes a second logic AND gate having a first input coupled to the output of said second channel signal processing element, a second input coupled to the output of said second logic gate, and an output coupled for transmitting the second channel of the output signal.

3. The signal modulation circuit of claim 1, said first channel signal processing element comprising:
a first delay gate having an input and an output coupled to the input and the output, respectively, of said first channel signal processing element;
a second delay gate having an input coupled to the input of said first channel signal processing element and an output;
a first storage element having a first input and a second input coupled to the input and the output, respectively, of said first delay gate, and an output;
a second storage element having a first input and a second input coupled to the outputs of said first delay gate and said second delay gate, respectively, and an output; and
a logic gate having a first input and a second input coupled to the outputs of said first and second storage elements, respectively, and an output coupled to the control signal output of said first channel signal processing element.

4. The signal modulation circuit of claim 1, wherein said first logic gate includes a logic AND gate and said second logic gate includes a logic NAND gate.

5. The signal modulation circuit of claim 1, said second channel signal processing element comprising:
a first delay gate having a first delay time and having an input coupled to the input of said second channel signal processing element and an output coupled to the output of said second channel signal processing element;
a second delay gate having a second delay time different from the first delay time and having an input coupled to the input of said second channel signal processing element and an output;
a first bistable gate having a data input coupled to the input of said second channel signal processing element, a reset input coupled to the output of said first delay gate, and an inverted output;
a second bistable gate having a first input coupled to the output of said first delay gate, a second input coupled to the output of said second delay gate, and an inverted output; and
a logic AND gate having a first input coupled to the inverted output of said first bistable gate, a second input coupled to the inverted output of said second bistable gate, and an output coupled to the control signal output of said second channel signal processing element.

6. The signal modulation circuit of claim 5, said second channel signal processing element further comprising:
a first inverter coupled between the input of said second channel signal processing element and the data input of said first bistable gate; and

a second inverter coupled between the output of said first delay gate and the reset input of said first bistable gate.

7. The signal modulation circuit of claim 1, further comprising a zero differential mode signal detection element having first and second inputs coupled to the outputs of said first and second channel signal processing elements, respectively, and an output coupled to said second logic gate.

8. A nonlinear amplifier, comprising:
a transform logic circuit coupled for receiving a differential signal and including:
a logic AND gate coupled for receiving the differential signal and configured to generate an output signal at an output thereof and at a first logic level in response to first and second components of the differential signal being at the first logic level;
a first processing element and a second processing element, each coupled for receiving a corresponding component of the differential signal and configured to generate a corresponding control signal at the first logic level and switching to a second logic level for a predetermined time interval following a rising edge and preceding a falling edge in the corresponding component of the differential signal; and
a switching element having first and second inputs coupled for receiving a corresponding component of the differential signal and first and second outputs, said switching element being conductive between the first input and output and between the second input and output in response to at least one of the first control signal, the second control signal, and the output signal of said logic AND gate being at the second logic level; and
a switching bridge having first and second control terminals coupled to the first and second outputs, respectively, of said switching element in said transform logic circuit.

9. The nonlinear amplifier of claim 8, wherein each of said first processing element and said second processing element in said transform logic circuit includes:
a first delay gate having a first delay time and having an input coupled for receiving a corresponding component of the differential signal and an output coupled to a corresponding input of said switching element;
a second delay gate having a second delay time and having an input coupled to the input of said first delay gate and an output;
a first bistable gate having a first input coupled to the input of said first delay gate, a second input coupled to the output of said first delay gate, and an output;

a second bistable gate having a first input coupled to the output of said first delay gate, a second input coupled to the output of said second delay gate, and an output; and

an AND gate having a first input coupled to the output of said first bistable gate, a second input coupled to the output of said second bistable gate, and an output.

10. The nonlinear amplifier of claim 9, wherein each of said first processing element and said second processing element in said transform logic circuit further includes a first inverter coupled between the input of said first delay gate and the first input of said first bistable gate and a second inverter coupled between the output of said first delay gate and the second input of said first bistable gate.

11. The nonlinear amplifier of claim 9, wherein said switching element in said transform logic circuit includes:

a logic NAND gate having a first input coupled to the output of said AND gate in said first processing element, a second input coupled to the output of said AND gate in said second processing element, a third input coupled to the output of said logic AND gate, and an output;

a first AND gate having a first input coupled to the output of said first delay gate in said first processing element, a second input coupled to the output of said logic NAND gate, and an output coupled to the first control terminal of said switching bridge; and

a second AND gate having a first input coupled to the output of said first delay gate in said second processing element, a second input coupled to the output of said logic NAND gate, and an output coupled to the second control terminal of said switching bridge.

12. The nonlinear amplifier of claim 11, said transform logic circuit further including a zero signal detection element having first and second inputs coupled to the outputs of said first delay gates in said first and second processing elements, respectively, and an output coupled to said logic NAND gate.

13. The nonlinear amplifier of claim 9, wherein:

the first delay time of said first delay gate in each of said first processing element and said second processing element in said transform logic circuit is substantially equal to the predetermined time interval; and

the second delay time of said second delay gate each of said first processing element and said second processing element in said transform logic circuit is substantially equal to twice of the predetermined time interval.

14. The nonlinear amplifier of claim 8, said switching bridge including:

a first switch having a control electrode coupled to the first output of said switching element in said transform logic circuit, a first current conducting electrode coupled to a first voltage level, and a second current conducting electrode coupled to a first output terminal of the nonlinear amplifier;
a second switch having a control electrode coupled to the control electrode of said first switch, a first current conducting electrode coupled to a second voltage level, and a second current conducting electrode coupled to the second current conducting electrode of said first switch;
a third switch having a control electrode coupled to the second output of said switching element in said transform logic circuit, a first current conducting electrode coupled to the first voltage level, and a second current conducting electrode coupled to a second output terminal of the nonlinear amplifier; and
a fourth switch having a control electrode coupled to the control electrode of said third switch, a first current conducting electrode coupled to the second voltage level, and a second current conducting electrode coupled to the second current conducting electrode of said third switch.

15. The nonlinear amplifier of claim 14, wherein:
said first switch includes a first pull-up field effect transistor;
said second switch includes a first pull-down field effect transistor;
said third switch includes a second pull-up field effect transistor; and
said fourth switch includes a second pull-down field effect transistor.

16. A signal modulation process, comprising the steps of:
providing a differential signal having a first channel and a second channel;
generating a first control signal and a second control signal at a first logic level;
switching the first control signal to a second logic level for a predetermined time interval following a rising edge and preceding a falling edge in the first channel of the differential signal;
switching the second control signal to the second logic level for the predetermined time interval following a rising edge and preceding a falling edge in the second channel of the differential signal; and
generating a modified signal by blocking a transmission of the differential signal in response to the first and second channels of the differential signal being at logic high and the first and second control signals at the first logic level.

17. The signal modulation process of claim 16, wherein the step of switching the first control signal to a second logic level for a predetermined time interval following a rising edge and preceding a falling edge in the first channel of the differential signal further includes the steps of:
generating a first delayed signal by delaying the first channel of the differential signal by the predetermined time interval;

generating a second delayed signal by delaying the first channel of the differential signal by two times of the predetermined time interval;
generating a first logic signal and a second logic signal at the first logic level;
in response to a rising edge in the first delayed signal, switching the first logic signal to the second logic level;
in response to a rising edge in the second delayed signal, switching the first logic signal back to the first logic level;
in response to a falling edge in the first channel of the differential PWM, switching the second logic signal to the second logic level;
in response to a falling edge in the first delayed signal, switching the second logic signal back to the first logic level; and
generating the first control signal at the first logic level in response to the first logic signal and the second logic signal at the first logic level and at the second logic level in response to at least one of the first logic signal and the second logic signal at the second logic level.

18. The signal modulation process of claim 17, wherein the step of generating a modified signal further includes the steps of:
generating a third control signal at the first logic level in response to the first delayed signal corresponding to the first channel of the differential signal and a first delayed signal corresponding to the second channel of the differential signal at the first logic level and at the second logic level in response to at least one of the first delayed signals corresponding to the first and second channels of the differential signal at the second logic level;
transmitting the first delayed signals corresponding to the first and second channels of the differential signal in response to at least one of the first, second, and third control signals at the second logic level; and
blocking the first delayed signals corresponding to the first and second channels of the differential signal in response to the first, second, and third control signals at the first logic level.

19. The signal modulation process of claim 16, wherein the step of generating a modified signal further includes the step of blocking the differential signal in response to a difference between the first and second channels of the differential signal being less than a predetermined value.

20. The signal modulation process of claim 16, further comprising the step of transmitting the modified signal to a switching bridge in a nonlinear amplifier.